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CLAIMS

[Claim(s)]
[Claim 1] The Horizontal Synchronizing signal distinction circuit characterized by including the circuit which distinguishes the polarity of a Horizontal Synchronizing signal with the composite synchronizing signal based on a broadcasting standard, and the circuit which outputs the Horizontal Synchronizing signal which chose the above-mentioned Horizontal Synchronizing signal or its reversal signal based on this result, and was made into the fixed polarity, and to choose.
[Claim 2] The circuit which distinguishes the polarity of the above-mentioned Horizontal Synchronizing signal is a Horizontal Synchronizing signal distinction circuit of claim 1 characterized by forming the selection signal which distinguishes the polarity of a Horizontal Synchronizing signal to the falling timing of a composite synchronizing signal, detects a vertical-synchronization period from the output and Horizontal Synchronizing signal, incorporates and holds the polar distinction signal of the above-mentioned Horizontal Synchronizing signal to the timing of a back edge, and chooses the above-mentioned Horizontal Synchronizing signal or its reversal signal.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention is used for the actuation circuit which distinguishes automatically the polarity of the Horizontal Synchronizing signal included in the composite synchronizing signal according to broadcasting formats, such as NTSC, and PAL, SECAM, concerning a Horizontal Synchronizing signal distinction circuit, and drives a solid state image pickup device, and relates to an effective technique.
[0002]
[Description of the Prior Art] The Horizontal Synchronizing signal changes in pulse width, a polarity, etc. with synchronizing signal generating circuits to pulse width, a polarity, etc. being decided by the broadcasting standard, as for a composite synchronizing signal. For this reason, it is necessary to limit the synchronizing signal generating circuit to be used and to perform a circuit design in the actuation circuit which generates the timing signal for inputting these synchronizing signals and driving a solid state image pickup device. Moreover, in giving

versatility, there is **** need independently about the Horizontal Synchronizing signal input only for straight polarity, and the input only for negative polarity. About solid-state imaging technique, there is issuance "a CCD camera technique" on Radio Technical company November 3, Showa 61, for example.

[0003]

[Problem(s) to be Solved by the Invention] In recent years, IC (semiconductor integrated circuit equipment) of the circumference circuit which the miniaturization of a video camera etc. progresses and drives a solid state image pickup device also has an indispensable miniaturization. For this reason, in such an IC for actuation, the cutback of the number of pins is indispensable in narrow-izing of a pin pitch. The object of this invention is to offer the Horizontal Synchronizing signal distinction circuit which enabled the cutback of versatility and the number of input terminals. The other objects and the new description will become clear from description and the accompanying drawing of this description along [said] this invention.

[0004]

[Means for Solving the Problem] It will be as follows if the outline of a typical thing is briefly explained among invention indicated in this application. That is, the polarity of a Horizontal Synchronizing signal is distinguished with the composite synchronizing signal based on a broadcasting standard, and the Horizontal Synchronizing signal which chose the above-mentioned Horizontal Synchronizing signal or its reversal signal based on this result, and was made into the fixed polarity is made to output.

[0005]

[Function] According to the above-mentioned means, since a desired polar Horizontal Synchronizing signal can be acquired irrespective of the polarity of the inputted Horizontal Synchronizing signal, versatility can be planned, without making the number of input terminals increase.

[0006]

[Example] The block diagram of one example of the Horizontal Synchronizing signal distinction circuit concerning this invention is shown in drawing 1 . Although each circuit block of this drawing is not especially restricted by the manufacturing technology of a well-known semiconductor integrated circuit, it is formed on one semi-conductor substrate with the circuit block which constitutes the actuation circuit which generates the various timing signals which drive a solid state image pickup device.

[0007] The Horizontal Synchronizing signal distinction circuit of this example consists of the **** distinction section, the latch section, the latch timing generating section, and the **** selection section. The polar distinction section is used on the basis of the composite synchronizing signal SYNC based on a broadcasting standard, and distinguishes the polarity of Horizontal Synchronizing signal HD formed of the Horizontal Synchronizing signal generating circuit which becomes various in each manufacturer etc. However, in a vertical-synchronization period, since polar distinction is reversed under the effect of an equivalence pulse, in order to eliminate this effect, the latch timing generating section and the latch section are prepared. The polar selection section wins popularity with Horizontal Synchronizing signal HD and the output signal of the inverting circuit which reverses this Horizontal Synchronizing signal HD, and makes any 1 way choose and output. The output signal of this polar selection section is used in order to form a clock pulse required for actuation of level CCD of a CCD solid state image pickup device, or the level shift register of an MOS form solid state image pickup device.

[0008] The concrete circuit diagram of one example of the above-mentioned Horizontal

Synchronizing signal distinction circuit is shown in drawing 2 . In drawing 3 , the timing chart of ** explaining actuation in case Horizontal Synchronizing signal HD is negative polarity is shown, and the timing chart of ** explaining actuation in case Horizontal Synchronizing signal HD is straight polarity is shown in drawing 4 at it.

[0009] In drawing 2 The polar distinction section is constituted by the flip-flop DF 1. An inverter circuit N1 is reversed and a composite synchronizing signal SYNC is supplied to the clock terminal C of this flip-flop DF 1. Horizontal Synchronizing signal HD is supplied to the data terminal D. Thereby, a flip-flop DF 1 incorporates Horizontal Synchronizing signal HD by the falling edge of a composite synchronizing signal SYNC, as shown in drawing 3 or drawing 4 . In this polar distinction section, a polarity can be distinguished by incorporation of Horizontal Synchronizing signal HD in the above timing. However, since the phenomenon in which a polarity will be reversed under the effect of an equivalence pulse in a vertical-synchronization period arises, this polar distinction output cannot be used as it is.

[0010] In this example, in order to prevent the inversion of the distinction result in this vertical-synchronization period, the pulse for every field is generated in the latch timing generating section, a ** field latch is carried out to the timing just behind an equivalence pulse, and a polar distinction result is outputted. The pulse output of the negative polarity which chose HD pulse polarity in the polar selection section by this distinction result, and was unified irrespective of the polarity of HD pulse to input is obtained. In order to eliminate the effect of ******** and the above equivalence pulses, the latch timing generating section is prepared, a vertical-synchronization period is detected, and it is made to make the output signal 1 of the above-mentioned polar distinction section hold by the back edge. The latch timing generating section consists of two flip-flops DF2 and DF3 and not-and (NAND) gate circuits NA1. Horizontal Synchronizing signal HD is supplied to the clock terminal C of a flip-flop DF 2, and Horizontal Synchronizing signal HD reversed by the inverter circuit N2 is supplied to the clock terminal C of a flip-flop DF 3. The output signal Q of the flip-flop DF 1 of the above-mentioned polar distinction section is supplied to the data terminal D of the above-mentioned flip-flops DF2 and DF3 in common.

[0011] Thereby, when Horizontal Synchronizing signal HD is negative polarity, the output 3 of a flip-flop DF 3 changes high-level in a vertical-synchronization period to the output 2 of a flip-flop DF 2 being fixed high-level, as shown in drawing 3 . So, the NAND gate circuit NA1 forms the output signal 4 which operated as an inverter circuit substantially and reversed the output signal 3 of a flip-flop DF 3. Moreover, when Horizontal Synchronizing signal HD is straight polarity, the output 2 of a flip-flop DF 3 changes high-level in a vertical-synchronization period to the output 2 of a flip-flop DF 3 being fixed high-level, as shown in drawing 4 . So, the output signal 4 of the NAND gate circuit NA1 is made into the reversal signal of the output signal 3 of a flip-flop DF 2. Thus, actuation which detects a vertical-synchronization period is performed in the latch timing generating section.

[0012] In drawing 2 , the latch section consists of flip-flops DF 4, the output signal 4 of the NAND gate circuit NA1 which is the output of the latch timing generating section is supplied to the clock terminal C, and the output signal 1 of the flip-flop DF 1 which is the output of the polar distinction section is supplied to the data terminal D. If this puts in another way synchronizing with the back edge of a Vertical Synchronizing signal period as shown in drawing 3 or drawing 4 , the polar distinction signal of Horizontal Synchronizing signal HD immediately after completing a Vertical Synchronizing signal will be held at the flip-flop DF 4 of the latch section.

[0013] In drawing 2 , the selection section consists of switch gate circuits which consist of

NAND gate circuits NA2-NA4. The outputs QB and Q of the flip-flop DF 4 of the latch section are supplied to one input of the NAND gate circuits NA2 and NA3, respectively. Horizontal Synchronizing signal HD reversed by the inverter circuit N3 is supplied to the input of another side of the NAND gate circuit NA2, and Horizontal Synchronizing signal HD is inputted into the input of another side of the NAND gate circuit NA3 as it is. The NAND gate circuit NA4 which receives the output signal of these NAND gate circuits NA2 and NA3 operates as an OR gate circuit substantially, and outputs the polar Horizontal Synchronizing signal chosen by the distinction result output 5. The **** example of a circuit is shown in drawing 2. About HD pulse **** distinction actuation by the circuit of drawing 2, it is ** [0014]. For example, if the high level H of the latch section is incorporated like drawing 3 , the NAND gate circuit NA3 will make Horizontal Synchronizing signal HD which opened the gate and was inputted choose and output. If the high level L of the latch section is incorporated like drawing 4 , Horizontal Synchronizing signal HD with which the NAND gate circuit NA2 opened the gate, and was reversed will be made to choose and output. That is, in this example, even if Horizontal Synchronizing signal HD inputted from the outside is either negative or forward, Horizontal Synchronizing signal HD supplied to an internal circuitry is unified into the pulse of negative polarity. Thereby, in order to give versatility, there is no **** need independently like before about the Horizontal Synchronizing signal input only for straight polarity, and the input only for negative polarity.

[0015] The operation effectiveness acquired from the above-mentioned example is as follows. Namely, (1) Since a desired polar Horizontal Synchronizing signal can be acquired irrespective of the polarity of the Horizontal Synchronizing signal inputted by making the Horizontal Synchronizing signal which distinguished the polarity of a Horizontal Synchronizing signal with the composite synchronizing signal based on a broadcasting standard, chose the above-mentioned Horizontal Synchronizing signal or its reversal signal based on this result, and was made into the fixed polarity output, the effectiveness that versatility can be planned is acquired without making the number of input terminals increase.

(2) The effectiveness that the cutback of the versatility of a circumference circuit and the number of IC pins which drive a solid state image pickup device corresponding to the miniaturization of a video camera etc. is realizable with the above (1) is acquired.

[0016] Although invention made by this invention person above was concretely explained based on the example, it cannot be overemphasized that it can change variously in the range which this invention is not limited to the above-mentioned example, and does not deviate from the summary. For example, as long as a level judging to the above edge timing is possible for the circuit which distinguishes a Horizontal Synchronizing signal and a polarity using a composite synchronizing signal, it may be anything. Similarly, the latch timing generating section may also detect a vertical-synchronization period, and may become by **********. It cannot be overemphasized that an output signal may be what is unified into the Horizontal Synchronizing signal of straight polarity besides what is made into the Horizontal Synchronizing signal of negative polarity as mentioned above. This invention can be widely used as a Horizontal Synchronizing signal distinction circuit used for the digital circuit which operates by inputting a composite synchronizing signal (SYNC) and a Horizontal Synchronizing signal (HD) as mentioned above.

[0017]

[Effect of the Invention] It will be as follows if the effectiveness acquired by the typical thing among invention indicated in this application is explained briefly. That is, since a desired polar

Horizontal Synchronizing signal can be acquired irrespective of the polarity of the Horizontal Synchronizing signal inputted by making the Horizontal Synchronizing signal which distinguished the polarity of a Horizontal Synchronizing signal with the composite synchronizing signal based on a broadcasting standard, chose the above-mentioned Horizontal Synchronizing signal or its reversal signal, and was made into the fixed polarity output, versatility can be planned, without making the number of input terminals increase.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram showing one example of the Horizontal Synchronizing signal distinction circuit concerning this invention.
[Drawing 2] It is the circuit diagram showing concrete 1 example of the Horizontal Synchronizing signal distinction circuit concerning this invention.
[Drawing 3] It is a timing chart for explaining an example of actuation of the Horizontal Synchronizing signal distinction circuit concerning this invention.
[Drawing 4] It is a timing chart for explaining other examples of actuation of the Horizontal Synchronizing signal distinction circuit concerning this invention.
[Description of Notations]
N1-N3 -- An inverter circuit, NA1-NA4 -- A NAND gate circuit, DF1-DF4 -- Flip-flop. HD -- A Horizontal Synchronizing signal, SYNC -- Composite synchronizing signal.